METHODS FOR FORMING SMALL-SCALE CAPACITOR STRUCTURES

TECHNICAL FIELD

[0001]   The present invention is related to methods for forming capacitors on microfeature workpieces, e.g., semiconductor substrates. Aspects of the invention have particular utility in connection with forming capacitors for use in microelectronic components, e.g., DRAM capacitors.

BACKGROUND

[0002]   Recent advances in the miniaturization of integrated circuits have led to smaller chip areas available for devices. High density dynamic random access memory chips (DRAMs), for example, leave little room for the storage node of a memory cell. Yet, the storage node (capacitor) must be able to store a certain minimum charge, determined by design and operational parameters, to ensure reliable operation of the memory cell. It is thus increasingly important that capacitors achieve a high stored charge per unit of chip area occupied.

[0003]   Traditionally, capacitors integrated into memory cells have structures based on the parallel plate capacitor. A layer of dielectric is disposed between two conductive layers and the layers are patterned, either sequentially during deposition or all at once. The patterned dielectric layer becomes the capacitor dielectric while the patterned conductive layers become the top and bottom plates or electrodes of the resultant capacitor structure. The charge stored on the capacitor is proportional to the capacitance (C) of the capacitor, $C = K\,K_0\,A/d$, where K is the dielectric constant of the capacitor dielectric, K_0 is the vacuum permittivity, A is the electrode area, and d is the spacing between electrodes.

[0004]   Several techniques have been developed to increase the total charge capacity of the cell capacitor without significantly affecting the chip area occupied

by the cell. These include increasing the effective surface area (A) of the electrodes by creating folding structures, such as trench or stacked capacitors. Such structures better utilize the available chip area by creating three-dimensional shapes to which the conductive electrodes and interlayer dielectric conform.

[0005]   One common way to increase the surface area of the capacitor electrodes employs a roughened or texturized electrode surface. U.S. Patent Application Publication 2003/0003697 to Agarwal et al. (the entirety of which is incorporated by reference), for example, suggests a roughened electrode surface that may comprise annealed ruthenium oxide. More conventionally, roughened polycrystalline silicon (commonly referred to as "polysilicon," or simply "poly") in the form of hemispherical grained polysilicon (commonly referred to as "HSG silicon" or "HSG polysilicon") has been used for a number of years as the bottom or storage electrode of microelectronic capacitors. Such bottom electrodes are commonly in contact with an active area of a silicon substrate that comprises part of a transistor. A thin dielectric layer is formed atop the bottom electrode and typically conforms reasonably well to the rough electrode surface. A top electrode may be deposited on the dielectric layer. The conformality of the dielectric layer commonly provides the outer surface of the dielectric layer with a roughened surface as well. The use of a rough bottom electrode, e.g., a layer of HSG polysilicon, thus effectively increases the electrode area (A in the capacitance formula above), which increases the capacitance of the capacitor structure.

[0006]   As a bottom electrode for a capacitor, however, roughened polysilicon is typically doped for conductivity to allow the bottom electrode to hold the requisite amount of charge. Unfortunately, rough polysilicon deposition techniques, such as HSG vacuum annealing, are most effective at lower doping levels. Further doping the polysilicon of the bottom electrode tends to result in diffusion of the dopants through the bottom electrode to the underlying active area of the substrate. For example, phosphorus from solid source P_2O_5, a commonly employed dopant, diffuses easily through silicon during high temperature anneal

steps. Downwardly diffused dopants can interfere with junction operation by changing the dopant profile of the active area and the transistor characteristics. Although some implanted dopants, such as arsenic ions, tend to diffuse more slowly, they may fail to adequately dope vertical surfaces, are often unduly expensive, and generally do not entirely eliminate the diffusion problem.

[0007]   Some have proposed depositing an electrically conductive layer on top of a HSG silicon bottom electrode. For example, U.S. Patent No. 6,211,033, issued to Sandhu et al. (the entirety of which is incorporated herein by reference), suggests depositing a layer of titanium nitride or titanium carbonitride on the outer surface of an HSG silicon electrode. The use of such a conductive overcoat can lead to greater conductivity in the bottom electrode with less doping of the HSG silicon layer and decreased diffusion of dopants. Such a titanium nitride or titanium carbonitride layer can also serve as an interface for high-stress locations in the HSG silicon layer, reducing the risk of cracking of the dielectric layer and the resultant current leakage. This Sandhu et al. patent suggests forming the titanium nitride or titanium carbonitride layer by metal organic chemical vapor deposition (MOCVD) employing tetrakis(dimethylamido)titanium (TDMAT) and a nitrogen carrier gas, or by CVD with a titanium halide, e.g., $TiCl_4$, as the titanium source and ammonia as the nitrogen source. Both of these CVD techniques can introduce significant levels of impurities in the resultant titanium nitride or titanium carbonitride film. Using MOCVD can incorporate carbon as an impurity in the form of titanium carbide. If the titanium nitride layer is instead deposited using titanium chloride and ammonia, chlorine atoms from the $TiCl_4$ can be incorporated in the deposited material and diffuse into the silicon.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008]   Figure 1 is a schematic representation of a system including a reactor for depositing a material on a single microfeature workpiece in accordance with select embodiments of the invention.

[0009]   Figure 2 is a schematic representation of a system including a reactor for depositing a material on surfaces of multiple microfeature workpieces in accordance with other embodiments of the invention.

[0010]   Figure 3 is a schematic illustration of one exemplary process for forming an electrically conductive layer in accordance with one aspect of the invention.

[0011]   Figure 4 is a schematic illustration of one exemplary process for forming another electrically conductive layer in accordance with another aspect of the invention.

[0012]   Figure 5 is a schematic illustration of an alternative process for forming an electrically conductive layer in accordance with still another aspect of the invention.

[0013]   Figure 6 schematically illustrates a first stage in the formation of a microelectronic capacitor in accordance with one embodiment of the invention.

[0014]   Figure 7 schematically illustrates the structure of Figure 5 and a subsequent stage of manufacture.

[0015]   Figure 8A is a schematic illustration of the structure of Figure 6 after addition of a first electrically conductive layer.

[0016]   Figure 8B is an enlarged close up view of the encircled area of Figure 7A.

[0017]   Figure 9A is a schematic illustration of the device of Figure 7A bearing another electrically conductive layer.

[0018]   Figure 9B is an enlarged isolation view of the encircled portion of Figure 8A.

[0019]   Figure 9C is an enlarged isolation view, similar to Figure 9B, of a portion of a device in accordance with another embodiment of the invention.

[0020]   Figure 9D is an enlarged isolation view, similar to Figure 9B, of a portion of a device in accordance with an alternative embodiment of the invention.

[0021]   Figure 10 is a schematic illustration of the device of Figure 6A bearing a dielectric layer.

[0022]   Figure 11 is a schematic illustration of the device of Figure 9 after addition of a second electrode layer.

[0023] Figure 12 is a schematic illustration of a microelectronic capacitor in accordance with one particular embodiment of the invention.

[0024] Figure 13 is a schematic illustration of a microelectronic capacitor in accordance with another embodiment of the invention.

[0025] Figure 14 is a schematic illustration of a microelectronic capacitor in accordance with still another embodiment of the invention.

DETAILED DESCRIPTION

A.   Overview

[0026] Various embodiments of the present invention provide methods of forming capacitors, e.g., capacitors employed as features of microelectronic components. Other embodiments of the invention provide microelectronic components that include capacitors. The term "microfeature workpiece" is used throughout to include substrates upon which and/or in which microelectronic devices, micromechanical devices, data storage elements, read/write components, and other features are fabricated. For example, microfeature workpieces can be semiconductor wafers such as silicon or gallium arsenide wafers, glass substrates such as borophosphosilicate glass (BPSG), and other types of materials. The microfeature workpieces typically have submicron features with dimensions of 0.05 microns or greater. Furthermore, the terms "gas" and "gaseous" are used throughout to include any form of matter that has no fixed shape and will conform in volume to the space available, which specifically includes vapors (i.e., a gas having a temperature less than the critical temperature so that it may be liquefied or solidified by compression at a constant temperature).

[0027] Several embodiments in accordance with the invention are set forth in Figures 1-14 and the following text to provide a thorough understanding of particular embodiments of the invention. A person skilled in the art will understand, however, that the invention may have additional embodiments, or that

the invention may be practiced without several of the details of the embodiments shown in Figures 1-14.

[0028]   One embodiment of the invention provides a method of fabricating a capacitor that includes forming a first electrode on a surface of a microfeature workpiece, forming a dielectric layer on the first electrode, and forming a second electrode over the dielectric layer. At least one of the first and second electrodes is formed by a) reacting a first gaseous precursor and a second gaseous precursor to deposit a first electrically conductive layer at a first deposition rate, and b) depositing a second electrically conductive layer at a second deposition rate that is less than the first deposition rate by depositing a precursor layer of a third gaseous precursor (which may be the same as the first precursor) at least one monolayer thick and exposing the precursor layer to a fourth gaseous precursor (which may be the same as the second precursor) to form a nanolayer reaction product. The second electrically conductive layer is in contact with the dielectric layer and may have a thickness of no greater than about 50Å.

[0029]   A method of fabricating a microelectronic capacitor in accordance with another embodiment of the invention includes depositing first and second conductive layers and, thereafter, depositing a dielectric layer and depositing an electrode on the dielectric layer. The first conductive layer is deposited at a first rate by reacting a first gaseous precursor and a second gaseous precursor in a first reaction process. The first conductive layer has a first surface roughness and a first impurity content. The second conductive layer is deposited at a second rate, which is slower than the first rate, by reacting the first gaseous precursor and the second gaseous precursor in a second reaction process. The second conductive layer has a second surface roughness that is smoother than the first surface roughness and a second impurity content that is lower than the first impurity content.

[0030]   A method of fabricating a microelectronic capacitor in accordance with another embodiment of the invention includes positioning a microfeature workpiece in a process chamber and forming an electrically conductive structure

on a surface of the microfeature workpiece. This surface may comprise a patterned layer of the microfeature workpiece or the surface of a previously-deposited layer or coating. This electrically conductive structure may be formed by sequentially depositing first, second, third, and fourth electrically conductive layers. The first electrically conductive layer is deposited by a first deposition process that comprises contemporaneously introducing a first gaseous precursor and a second gaseous precursor to the process chamber to form a first reaction product. The second electrically conductive layer is deposited on the first electrically conductive layer by a second deposition process. This second deposition process may comprise alternately introducing quantities of the first and second precursors to the process chamber to form at least two layers of a second reaction product. The third electrically conductive layer may be deposited on the second electrically conductive layer by the first deposition process outlined above, and the fourth electrically conductive layer may be deposited on the third electrically conductive layer by the second deposition process outlined above.

[0031]   Yet another embodiment of the invention provides a microelectronic component comprising a plurality of memory cells carried by a substrate. Each memory cell includes a capacitor that comprises a first electrode, a dielectric layer and a second electrode deposited on the dielectric layer. The first electrode includes, moving outwardly from a surface of the substrate, a hemispherical grain polycrystalline silicon layer, a layer of a bulk deposition product comprising a primary species, and a layer of a nanolayer deposition product comprising the same primary species. The layer of the nanolayer deposition product has a thickness of no greater than 50Å and the bulk deposition product has an impurity content higher than an impurity content of the nanolayer deposition product. The dielectric layer is deposited on the nanolayer deposition product of the first electrode.

[0032]   For ease of understanding, the following discussion is subdivided into two areas of emphasis. The first section discusses aspects of processing systems that may be used in accordance with selected embodiments of the invention. The

second section outlines methods in accordance with other aspects of the invention.

B.   Processing Systems

[0033]'   Figure 1 schematically illustrates a reactor 10 that may be used to form capacitors in accordance with select embodiments of the invention. The reactor 10 of Figure 1 includes a process chamber 20 coupled to a gas supply 30 and a vacuum 40. The reactor 10 may also include a heater plate 50 that supports the microfeature workpiece W and a gas dispenser 60, both of which are disposed in the process chamber 20. The gas dispenser 60 includes a plenum 62 operatively coupled to the gas supply 30 and a distributor plate 70 having a plurality of holes 72. In operation, the heater plate 50 may heat the workpiece W to a desired reaction temperature and the desired combination or series of gases may be injected into the process chamber 20 via the gas dispenser 60. The vacuum 40 can maintain a negative pressure in the process chamber 20 to draw the gases from the gas dispenser 60 across the workpiece W and then through an outlet in the process chamber 20.

[0034]   The gas supply 30 of the reactor 10 shown in Figure 1 includes a plurality of gas sources 31 (identified individually as 31a-c), a valve assembly 34 having a plurality of valves, and a plurality of gas supply lines 32 and 36. The gas sources 31 can include any number of gases anticipated to be needed for various reactions in the process chamber 20. In the particular embodiment shown schematically in Figure 1, the gas sources 31 include a first gas source 31a for providing a first gas, a second gas source 31b for providing a second gas, and a third gas source 31c for providing a third gas. In one example, the first and second gases can be first and second precursors, respectively, and the third gas can be a purge gas. As discussed in more detail below, the first and second precursors may be chemical species that react to form a reaction product on a surface of the microfeature workpiece W. The gas supply 30 can include more

gas sources 31 for other applications that require additional precursors or purge gases. For example, the first and second precursors may be used to deposit an electrically conductive layer or layers and an additional precursor or precursors may be provided in additional gas sources 31 (not shown) to deposit a dielectric layer as described below.

[0035]   The valve assembly 34 may be operated by a controller 38 that generates signals for controlling the flow of gases to the reaction chamber 20. In one embodiment, this controller 38 comprises a computer having a programmable processor programmed to control operation of the valve assembly 34 to deposit material on the workpiece W. If so desired, the controller 38 may also be coupled to the vacuum 40 and/or the heater 50 to further control the reaction conditions adjacent the surface of the workpiece W. For example, the controller 38 can be programmed to heat the workpiece to a desired temperature via the heater 50 and operate the valve assembly 34 to pulse quantities of different gases individually through the gas distributor 60 in atomic layer deposition (ALD) applications or mix selected precursors in the plenum 62 of the gas distributor 60 in continuous or pulsed CVD processes.

[0036]   The reactor 10 of Figure 1 is adapted to receive and process a single microfeature workpiece W in the process chamber 20. To increase throughput of CVD and ALD processes, the microelectronics industry, for example, is moving toward batch processing of workpieces W. Figure 2 schematically illustrates a reactor 12 adapted for batch processing of workpieces W. Many of the elements of this batch reactor 12 are similar to the reactor 10 of Figure 1 and like reference numbers are used to designate similar elements. In the embodiment of Figure 1, the workpiece W is supported on a heater plate 50 that is also adapted to heat the workpiece W. In the batch reactor 12, one or more workpieces W may be supported in the process chamber 20 by a workpiece holder 52. For example, the workpiece holder 52 may be adapted to hold anywhere from 20 to 250 microfeature workpieces W for concurrent processing. The microfeature

workpieces W may be heated during processing by one or more radiant heat panels 50 arranged about the periphery of the process chamber 20.

C.   Methods of Depositing Materials On Micro-Device Workpieces

[0037]   As noted above, other embodiments of the invention provide methods of forming capacitors, e.g., by forming a capacitor on a microfeature workpiece for use as a microelectronic capacitor. In the following discussion, reference is made to the processing system 10 shown schematically in Figure 1. It should be understood, though, that reference to this particular processing system is solely for purposes of illustration and that the methods outlined below are not limited to any particular processing system.

Deposition Techniques

[0038]   As discussed below, various embodiments of the invention employ both chemical vapor deposition (CVD) and atomic layer deposition (ALD). Both CVD and ALD, as used herein, involve the use of at least one chemical species that can decompose or can react with another chemical species to form a desired material on the workpiece W. Such chemical species are referred to herein as "precursors." One of the differences between a CVD process employing two or more precursors and an ALD precursor employing two or more precursors is the relative timing of the delivery of the precursors to the proximity of the workpiece W. In CVD processes, both of the precursors are simultaneously present in and react in a space adjacent the surface of the workpiece W; in conventional ALD processes, the precursors are introduced separately and primarily react directly on the surface of the workpiece W.

[0039]   CVD is commonly used to deposit a completed reaction product on a surface of a workpiece W. The conditions adjacent a workpiece surface may be used to catalyze a gas-phase reaction or decomposition of the precursor(s) to form a reaction product. This completed reaction product is deposited on the surface of the workpiece W. Commonly, both of the precursors in a two-precursor

CVD process are introduced contemporaneously, i.e., during an overlapping period of time.

[0040]   Figure 3 schematically illustrates a gas flow of a CVD process 100 in accordance with one embodiment of the invention as a plot of flow rate over time. In this process 100, a first gaseous precursor flow 101 and a second gaseous precursor flow 102 are contemporaneously delivered to the process chamber 20 of the reactor 10. This may be accomplished by controlling the valve assembly 34 to deliver the first precursor from the first gas source 31a and the second precursor from the second gas source 31b. Both of these gases are delivered to the plenum 62 of the gas dispenser 60, where they will at least begin to be mixed together. This mixture of gases can then be delivered to the proximity of the workpiece W by the distributor plate 70. In Figure 3, the first gas flow 101 and the second gas flow 102 are shown as starting and ending at substantially the same time. In other embodiments, the first gas flow 101 may start before or after the second gas flow 102 is initiated and the first gas flow 101 may be terminated before or after the second gas flow 102 is terminated. In each of these cases, the first gas flow 101 and the second gas flow 102 may be said to be contemporaneous if they occur simultaneously over a material period of time, i.e., they need not start and/or stop at the same time.

[0041]   Figure 3 schematically illustrates delivery of a purge/carrier gas. In this embodiment, the purge gas may be delivered before initiating the first and second gas flows 101 and 102 and again delivered to the process chamber 20 after the first and second gas flows 101 and 102 are terminated. Such a purge gas flow 103 may be used in conjunction with the vacuum 40 to purge any excess precursors from the process chamber 20. In other embodiments, the purge/carrier gas may be delivered contemporaneously with the first and second gaseous precursors, in which case it serves as a more conventional carrier gas to provide adequate gas flow through the dispenser 60 while controlling the concentration of the precursors in the gas flow. In the context of Figure 1, the third gas flow 103

may be delivered by selectively controlling the valve assembly 34 to deliver the purge gas from the third gas source 31c to the gas dispenser 60.

[0042]   Atomic layer deposition, in contrast with CVD, generally involves delivering precursors in alternating pulses rather than delivering them contemporaneously. Figure 4 is a schematic plot of gas flow rates as a function of time in accordance with an ALD process 110 in accordance with one embodiment of the invention. In this process 110, discrete quantities of the first gaseous precursor are delivered in first precursor pulses 111a and 111b. Discrete quantities of the second gaseous precursor are delivered to the process chamber 20 in second precursor pulses 112a and 112b. The first pulses 111 and second pulses 112 are delivered at different times in an alternating fashion.

[0043]   Moving down the timeline of Figure 4, one pulse 111a of the first precursor may be delivered to the process chamber 20 to contact the surface of the workpiece W. The precursor may be at least chemisorbed on the workpiece W. Theoretically, such chemisorbtion will form a monolayer that is uniformly one molecule thick on the entire surface of the workpiece W. Such a monolayer may be referred to as a saturated monolayer. As a practical matter, in some circumstances some minor portions of the workpiece surface may not chemisorb a molecule of the precursor. Nevertheless, such imperfect monolayers are still referred to herein as monolayers. In many applications, a substantially saturated monolayer may be suitable. A substantially saturated monolayer is a monolayer that will yield a deposited layer exhibiting the requisite quality and/or electrical properties.

[0044]   An excess of the first precursor is typically delivered to the process chamber 20. This excess first precursor can be purged from the vicinity of the workpiece surface. Purging may involve a variety of techniques, including any combination of contacting the substrate and/or monolayer with a purge gas and/or lowering pressure in the process chamber 20 to below the pressure needed to deposit the precursor on the workpiece surface. Examples of suitable carrier gases include nitrogen, argon, helium, neon, krypton, and xenon. In the particular

embodiment shown in Figure 4, a first pulse 113a of the purge gas is delivered to the process chamber 20 and a majority or all of this purge gas pulse 113a may take place after the first precursor pulse 111a is completed. The purge process shown in Figure 4 also includes a pump-down step 115a wherein the vacuum 40 will withdraw gas from the process chamber 20 without introducing any additional gas from the gas supply 30. The parameters of the purge pulse 113a and pump-down 115a may be determined experimentally, as known in the art. The pump-down time and/or the quantity of purge gas in the pulse 113a may be successively reduced until the film growth rate increases. Such an increase in film growth rate may be deemed an indication that excess quantities of the first precursor remain in the process chamber 20, which may be used to establish a minimum purge gas quantity and/or purge time.

[0045]   Once the process chamber 20 has been suitably purged, a pulse 112a of the second gaseous precursor may be delivered to the process chamber 20. This second precursor may chemisorb on the first monolayer of the first precursor and/or react with the monolayer to form a reaction product. This reaction product is typically one or no more than a few molecules thick, yielding a very thin, highly conformal nanolayer reaction product. After a suitable exposure to the second gaseous precursor, the second precursor pulse 112a may be terminated and the process chamber 20 may be purged again with a pulse 113b of purge gas and/or a pump-down step 115b.

[0046]   As suggested in Figure 4, the pair of precursor pulses 111a and 112a, together with the associated pulses 113a and 113b of purge gas and/or pump-down steps 115a and 115b, may be considered one cycle. This cycle will form a nanolayer that is usually thinner than the desired total thickness, with typical thicknesses of just 1 or 2 molecules (e.g., less than 1 nm, often less than 2Å). As a consequence, the cycle is often repeated numerous times to yield a layer with an appropriate thickness. Hence, Figure 4 illustrates a second cycle that involves delivering a further pulse 111b of the first precursor, purging the process chamber 20 with a further purge gas pulse 113c and pump-down 115c, subsequently

delivering another second precursor pulse 112b, and again purging the process chamber 20 with another purge gas pulse 113d and pump-down 115d. This process can be repeated as many times as necessary to yield a layer of the desired thickness.

[0047]   Figure 5 schematically illustrates a gas flow profile analogous to Figure 4, but illustrating a process 120 in accordance with another embodiment of the invention. In this process 120, pulses 121a-d of the first gaseous precursor are alternated with pulses 122a-d of the second gaseous precursor. This is similar in some respects to the pulses 111 and 112 illustrated in Figure 4 in the process 120 shown in Figure 5. However, there is no purge process (e.g., purge pulse 113a and pump-down 115a in Figure 4) between delivery of successive quantities of the first and second precursors. Hence, in Figure 5, the first pulse 122a of the second gaseous precursor may immediately follow completion of the first pulse 121a of the first gaseous precursor. Likewise, the next pulse 121b of the first precursor may immediately follow termination of the first pulse 122a of the second precursor. In this process, a monolayer of the first precursor may be deposited on the surface of the workpiece prior to delivery of the pulse of the second precursor. Without the purge phase, though, some of the first precursor may remain in the vicinity of the workpiece W when the next pulse of the second gaseous precursor is initiated. This may result in a gaseous phase reaction between the precursors in a gaseous, unbound phase, leading to direct deposition of the reaction product on the surface of the workpiece W, and an increase in the rate of film formation. By appropriately selecting the process conditions and the timing of the pulses 121 and 122, though, this CVD-like secondary deposition may be held in check and may not significantly adversely affect the quality of the ALD-deposited material.

[0048]   In other embodiments, the process chamber 20 may be purged between some, but not all, precursor pulses. For example, one pulse (e.g., 121a) of the first precursor and one pulse (e.g., 122a) of the second precursor may form one cycle of material deposition. A purge step, which may comprise delivery of a purge gas and/or a pump-down of the process chamber 20, may be performed

between cycles to better promote deposition of a monolayer of the first precursor on the layer of material deposited in the previous cycle.

[0049]   The process 120 shown in Figure 5 may not technically conform to conventional definitions of atomic layer deposition because remnants of one precursor are present when the subsequent precursor is introduced. Nonetheless, it is anticipated that such a "pseudo-ALD" process may deliver many of the benefits desired from ALD layers in accordance with select methods outlined below. As a consequence, the term "ALD" is used herein to refer to both conventional ALD, (e.g., deposition via the process 110 illustrated in Figure 3) and "pseudo-ALD" (e.g., deposition via the process 120 shown in Figure 4).

[0050]   Under most CVD conditions, the reaction between the precursors occurs largely independently of the composition or surface properties of the workpiece on which the reactant is being deposited. By contrast, the chemisorbtion rate of a precursor in ALD may be influenced by the composition, crystalline structure, and other properties of the workpiece surface, including any previously chemisorbed chemical species on that surface. If necessary, the surface of the workpiece can be prepared before ALD to enhance the deposition of the monolayer of the first precursor. For example, if an ALD layer is to be formed on HSG silicon, it may be advantageous to expose the HSG silicon to water vapor to provide –OH termination at the surface.

[0051]   ALD and CVD processes each have some advantages and disadvantages. The primary advantage of CVD in the context of the present invention is that it may deposit material at a significantly higher rate than ALD processes. Whereas CVD techniques may require only about one minute to form a 60Å thick layer, for example, ALD techniques using analogous precursors may take several minutes to form a layer having the same thickness by depositing a series of nanolayers. In single-wafer processing chambers, ALD processes can take 500-2000 percent longer than corresponding single-wafer CVD processes.

[0052]   Although ALD may take appreciably longer than CVD, materials deposited via ALD are often superior in a number of respects to analogous materials

deposited via CVD. For example, building up a layer of ALD material as a series of independently deposited nanolayers can yield significantly higher conformality to underlying surface roughness than is typically achieved using CVD with the same precursors. Layers deposited via CVD also tend to include a significantly higher concentration of impurities than an analogous material deposited via ALD. As noted above in connection with U.S. Patent No. 6,211,033, depositing titanium nitride or titanium carbonitride via MOCVD (e.g., TDMAT/nitrogen) or CVD (e.g., $TiCl_4/NH_3$) can incorporate undesirable amounts of carbon and/or chlorine in the resultant layer. The crystallinity and crystal habit of the layer deposited via CVD will vary depending on the process conditions, but the grain size in crystalline CVD films is often larger than any grains that may develop in ALD films. This tends to produce a rougher surface on CVD-deposited layers than on analogous ALD-deposited layers. Particularly if the dielectric is not deposited in a highly conformal deposition process, this microroughness of CVD layers may adversely impact the quality of the electrical interface between a CVD-deposited electrode and an overlying dielectric layer.

Manufacturing Processes

[0053]   Figures 6-11 schematically illustrate sequential stages in the manufacture of a microelectronic capacitor 200 in accordance with one embodiment of the invention. Turning first to Figure 6, the workpiece W shown in this drawing includes a semiconductor substrate 202 having a heavily doped active area 208. An electrically insulating layer 204 is carried by the substrate 202 and has an opening 206 that extends from an exterior of the insulating layer 204 down to the active area 208 of the substrate 202. This provides the workpiece W with a three-dimensional outer surface S upon which materials will be deposited in subsequent steps. A workpiece W such as that shown in Figure 6 may be made easily using conventional techniques known in the art.

[0054]   In Figure 7, a hemispherical grain polysilicon layer 210 has been formed on the surface S of the workpiece W of Figure 6. The HSG silicon layer 210 has

a rough surface 212 that increases the surface area of the layer, as discussed above. As discussed below, this HSG silicon layer 210 may define a layer of a bottom electrode of the capacitor 200. If so desired, the HSG silicon layer 210 may be doped, e.g., with arsenic or phosphorous, to enhance its electrical conductivity. The HSG silicon layer 210 may be formed in any of a variety of commonly known methods. One such method includes vacuum annealing of an amorphous silicon layer or a polysilicon layer with relatively small grain size, inducing grain growth at nucleation sites. Another common method of forming HSG silicon includes direct deposition, wherein polysilicon selectively grows at nucleation sites during deposition.

[0055]   Figures 8A and 8B schematically illustrate the workpiece W of Figure 7 after deposition of an electrically conductive CVD layer 220 on the rough surface 212 of the HSG silicon layer 210. The CVD layer 220 may be deposited in any of a variety of CVD processes that will yield an electrically conductive layer 220 that conforms reasonably well to the roughened surface 212 of the HSG polysilicon. In certain embodiments of the invention, the CVD layer 220 is deposited by introducing a first gaseous precursor and a second gaseous precursor to the process chamber 20 of the reactor 10 at the same time so these gases may react and be deposited directly on the surface 212 of the HSG layer 210. In one exemplary embodiment, the CVD layer 220 comprises a layer of titanium nitride formed by reaction of a titanium-containing first precursor and a nitrogen-containing second precursor. For example, a titanium nitride CVD layer 220 may be deposited by introducing titanium chloride $TiCl_4$ and NH_3 to the process chamber 20 under appropriate conditions, which are widely known. In another embodiment employing MOCVD, TDMAT is used as a metal organic precursor and nitrogen is used as a carrier gas. As suggested in Figure 8B, the outer surface 222 of the CVD layer 220, i.e., the surface of the CVD layer 220 spaced away from the underlying HSG silicon layer 210, may exhibit microroughness, illustrated schematically in Figure 8B as an irregular outer surface 222.

[0056]   As illustrated in Figures 9A and 9B, an ALD layer 230 may be deposited on the outer surface 222 of the CVD layer 220. This ALD layer may be formed using any suitable ALD technique, including, but not limited to, the ALD processes 110 and 120 shown in Figures 4 and 5, respectively. This ALD layer 230 will typically comprise at least two nanolayers, with each nanolayer being generated in a single cycle of the ALD process. Both the combined thickness of the CVD layer 220 and the ALD layer 230 and the relative thicknesses of these layers 220 and 230 may vary depending on the material used and the desired capacitance of the capacitor 200. In one embodiment, the combined thickness of the CVD layer 220 and the ALD layer 230, referred to collectively as an electrically conductive coating (225 in Figure 9B), may be on the order of about 50-500Å, e.g., about 150-250Å. In certain embodiments of the invention, the ALD layer 230 has a thickness of no greater than 50Å, with the balance of the electrically conductive coating 225 comprising the CVD layer 220.

[0057]   The ALD layer 230 may be formed of an electrically conductive material having a primary species that is different from a primary species of the electrically conductive material of the CVD layer 220. In many embodiments of the present invention, though, the ALD layer 230 and the CVD layer 220 comprise the same primary species (e.g., TiN). As noted above, though, the CVD layer 220 likely will have a higher impurity content, (e.g., TiC or chlorine) than will the ALD layer 230. In one particular embodiment, the precursors used to deposit the CVD layer 220 are the same precursors used to deposit the ALD layer 230. In other embodiments wherein the CVD layer 220 and the ALD layer 230 generally comprise the same primary species, the CVD layer may be formed using one precursor or a pair of precursors and the ALD layer 230 may be formed using a different precursor or pair of precursors.

[0058]   The electrically conductive coating 225 shown in Figures 9A-B comprises a single CVD layer 220 and a single ALD layer 230. In other embodiments, however, the electrically conductive coating 225 may comprise three or more layers. As suggested in Figure 9C, for example, this electrically conductive

coating 225 may comprise an initial ALD layer 230a deposited directly atop the roughened surface 212 of the HSG silicon, a CVD layer 220 may be deposited on that initial ALD layer 230a, and an outer ALD layer 230b may be deposited on the irregular surface 222 of the CVD layer 220. In another embodiment, illustrated in Figure 9D, the electrically conductive coating comprises an ALD layer 231 deposited on the surface 212 of the HSG silicon and a CVD layer 220 on the ALD layer, with the dielectric layer (layer 240 in Figure 10) deposited on the CVD layer 220. For reasons noted below, the dielectric layer in select embodiments of the invention is deposited on or is otherwise in direct contact with a layer deposited via ALD, e.g., ALD layer 230.

[0059]   In another exemplary embodiment, the electrically conductive layer 225 atop the HSG silicon layer 210 comprises a first CVD-deposited layer, an ALD-deposited layer atop the first CVD-deposited layer, a second CVD-deposited layer atop the first ALD-deposited layer, and a second ALD-deposited layer deposited atop the second CVD-deposited layer. In other embodiments, the electrically conductive layer 225 comprises five or more layers, with the layers alternating between CVD-deposited layers and ALD-deposited layers. In still other embodiments, the HSG silicon layer 210 may be omitted and the electrically conductive layer 225 may be deposited directly on the surface S of the workpiece W shown in Figure 6. In such an embodiment, the electrically conductive layer 225 will form the entirety of the bottom electrode of the capacitor 200 of Figure 12. Such an electrically conductive layer may comprise three or more alternating ALD-deposited and CVD-deposited layers.

[0060]   The outer surface 232 of the ALD layer 230, i.e., the surface that is spaced away from the irregular surface 222 of the CVD layer 220, may be relatively smooth. As suggested in Figures 9A-B, this surface 232 likely will not be perfectly flat. On a localized scale, though, the ALD layer will have a surface roughness that is less than the surface roughness of the irregular surface 222 of the CVD layer 220. This smooth surface 232 is anticipated to provide a more effective

electrical contact between the electrically conductive coating and the subsequently-deposited dielectric layer 240, discussed below.

[0061]   Figure 10 schematically illustrates the workpiece W of Figure 9A after deposition of a dielectric layer 240. The HSG silicon layer 210, the CVD layer 220, and the ALD layer 230 shown in Figure 9A extend across much or all of the surface of the workpiece W. In one embodiment, the dielectric layer 240 is deposited on the structure and all four of the layers 210, 220, 230, and 240 may cover much if not all of the surface of the workpiece W. In the embodiment shown in Figure 10, though, the layers illustrated in Figure 9A have been patterned to remove excess material, leaving the surface of the opening 206 and, in one embodiment, a peripheral margin of the opening 206 covered. This may be accomplished using conventional photolithographic and selective etching techniques.

[0062]   A wide variety of dielectric materials suitable for use as the dielectric layer 240 are well known in the art of microelectronic capacitors. As noted in the background section above, the capacitance of a capacitor can be increased by increasing the dielectric constant of the dielectric material and/or reducing the thickness of the dielectric material. Although conventional silica (SiO_2) or silicon nitride (Si_3N_4) may be employed, materials with higher dielectric constants – including, for example, alumina (Al_2O_3), tantala (Ta_2O_5), barium strontium titanate (BST), strontium titanate (ST), barium titanate (BT), lead zirconium titanate (PZT), and strontium bismuth titanate (SBT) – may yield a capacitor 200 with a higher capacitance. In one specific example, the dielectric layer 240 comprises alumina. The dielectric layer may be deposited in any desired fashion, including CVD, ALD, or sputtering.

[0063]   Figure 11 schematically illustrates the workpiece W of Figure 10 after a second electrode 250 has been deposited on the dielectric layer 240. This second electrode 250 may be formed in any suitable manner. In one particular embodiment, the electrode 250 is formed via CVD. The material of the electrode 250 may be any electrically conductive material that is compatible with the

dielectric layer 240 and the other components of the workpiece W. In one particular embodiment, the electrode 250 comprises the same primary species as the primary species of the CVD layer 220 and/or the ALD layer 230. For example, if the CVD layer 220 and the ALD layer 230 comprise TiN, the electrode 250 may also comprise TiN. In one particular embodiment, the electrode 250 is formed using the same precursors and the same basic deposition process as those used to deposit the CVD layer 220 and/or the ALD layer 230.

[0064]   Figure 12 illustrates the finished capacitor 200. In forming the finished capacitor 200, the surface of the workpiece W shown in Figure 11 may be patterned using conventional photolithographic and etching techniques.

[0065]   Methods in accordance with the present invention may be employed to create capacitors having a variety of different structures. For example, Figure 13 illustrates a microelectronic capacitor 200a in accordance with an alternative embodiment of the invention. Many of the elements of Figure 12 are shown in Figure 13, and like reference numbers are used in Figures 12 and 13 to indicate like elements. One difference between the electrodes 200 and 200a is the interface between the electrode 250 and the dielectric layer 240. In the capacitor 200, the electrode 250 may comprise a bulk layer of material formed, e.g., by a continuous CVD process. The capacitor 200a of Figure 13 instead employs a second ALD layer 270 on the outer surface of the dielectric layer 240, i.e., the surface of the dielectric layer 240 oriented away from the first ALD layer 230. This second ALD layer 270 may be deposited in much the same fashion as the first ALD layer 230. In select embodiments, the ALD layer 270 may have a thickness of no greater than about 50Å. Because of the highly conformal nature of ALD coatings, the addition of such a second ALD layer 270 is expected to improve the electrical interface between the dielectric 240 and the outer electrode 250.

[0066]   Figure 14 schematically illustrates a capacitor 200b in accordance with another embodiment of the invention. Like reference numbers are used in Figures 13 and 14 to indicate like elements. One difference between the

capacitors 200a and 200b is that the capacitor 200b of Figure 14 omits the first dielectric layer 230 employed in the capacitor 200a of Figure 13. Instead, a single ALD layer 270 is disposed between the dielectric layer 240 and the rest of the top electrode 250.

[0067] Further variations of these embodiments are also envisioned. For example, the majority of the thickness of the electrode 250 in each of the illustrated embodiments comprises a single bulk layer. In other embodiments of the invention, the electrode 250 may be formed as an alternating series of ALD-deposited and CVD-deposited layers.

[0068] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense as opposed to an exclusive or exhaustive sense, i.e., in a sense of "including, but not limited to." Words using the singular or plural number also include the plural or singular number, respectively. Use of the word "or" in the claims in reference to a list of items is intended to cover a) any of the items in the list, b) all of the items in the list, and c) any combination of the items in the list.

[0069] The above-detailed descriptions of embodiments of the invention are not intended to be exhaustive or to limit the invention to the precise form disclosed above. Specific embodiments of, and examples for, the invention are described above for illustrative purposes, but various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, whereas steps are presented in a given order, alternative embodiments may perform steps in a different order. The various embodiments described herein can be combined to provide further embodiments.

[0070] In general, the terms used in the following claims should not be construed to limit the invention to the specific embodiments disclosed in the specification, unless the above-detailed description explicitly defines such terms. While certain aspects of the invention are presented below in certain claim forms, the inventors contemplate the various aspects of the invention in any number of claim forms.

Accordingly, the inventors reserve the right to add additional claims after filing the application to pursue such additional claim forms for other aspects of the invention.